

Figure 1a: Single-Thread Processor. This figure shows a 40-cycle execution of a single-thread processor. The processor has a 40-cycle execution time. The execution is divided into four 10-cycle segments. The first segment (cycles 1-10) shows the processor executing a sequence of instructions: A, B, C, D, E, F, G, H, I, J. The second segment (cycles 11-20) shows the processor executing a sequence of instructions: A, B, C, D, E, F, G, H, I, J. The third segment (cycles 21-30) shows the processor executing a sequence of instructions: A, B, C, D, E, F, G, H, I, J. The fourth segment (cycles 31-40) shows the processor executing a sequence of instructions: A, B, C, D, E, F, G, H, I, J. The execution is divided into four 10-cycle segments. The first segment (cycles 1-10) shows the processor executing a sequence of instructions: A, B, C, D, E, F, G, H, I, J. The second segment (cycles 11-20) shows the processor executing a sequence of instructions: A, B, C, D, E, F, G, H, I, J. The third segment (cycles 21-30) shows the processor executing a sequence of instructions: A, B, C, D, E, F, G, H, I, J. The fourth segment (cycles 31-40) shows the processor executing a sequence of instructions: A, B, C, D, E, F, G, H, I, J.

Single-Thread Processor

machine cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40				
PC	A	B	C	D	E	E	E	E	E	E	E	F	F	F	F	F	F	F	G	G	G	H	H	H	H	H	H	H	I	I	I	I	I	J	J	J	J	J	J	J				
FETCH		A	B	C	D	D	D	D	D	D	D	E	E	E	E	E	E	E	F	F	F	F	G	G	G	G	G	H	H	H	H	H	I	I	I	I	I	I	I	I	I			
DECODE			A	B	C	C	C	C	C	C	C	D	D	D	D	D	D	D	E	E	E	E	F	F	F	F	F	F	F	F	F	F	F	G	G	H	H	H	H	H	H			
OPERAND			A	B	B	B	B	B	B	B	B	C	C	C	C	C	C	D	D	D	D	D	E	E	E	E	E	E	E	F	F	F	F	F	G	G	G	G	G	G	G			
EXECUTE				A							B						C						D						E					F										
ADDRESS					A		A					B		B				C		C				D		D			E		E				F		F							
MEM								A						B						C																								
MEM									A						B						C																							
MEM										A						B						C																						
WRITEBACK											A																																	
memory in use							1	1	1	1			1	1	1	1		1	1	1	1				1	1	1	1	1									1	1	1	1	1	1	

Figure 1a

Single-Thread Processor with Data Cache

machine cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40				
PC	A	B	C	D	E	E	E	E	F	F	G	G	G	H	H	H	I	I	I	J	J	J	K	K	K	L	L	L	L	M	M	M	N	N	N	O	O	P	P	P	P			
FETCH		A	B	C	D	D	D	D	E	E	E	F	F	F	G	G	H	H	H	I	I	J	J	J	K	K	K	L	L	L	M	M	M	N	N	N	O	O	O	O	O	O		
DECODE			A	B	C	C	C	C	D	D	D	D	D	E	E	F	F	F	G	G	G	H	H	H	I	I	I	J	J	J	K	K	K	L	L	L	M	M	M	N	N	N	N	
OPERAND				A	B	B	B	B	B	B	C	C	D	D	D	E	E	F	F	F	G	G	G	H	H	H	I	I	I	J	J	J	K	K	K	L	L	L	M	M	M	M	M	M
EXECUTE					A					B					D		E	E	E	F	F	F	G	G	G	H	H	H																
ADDRESS					A					B					D		E	E	E	F	F	F	G	G	G	H	H	H																
WRITEBACK										B					D		E	E	E	F	F	F	G	G	G	H	H	H																

Figure 1b

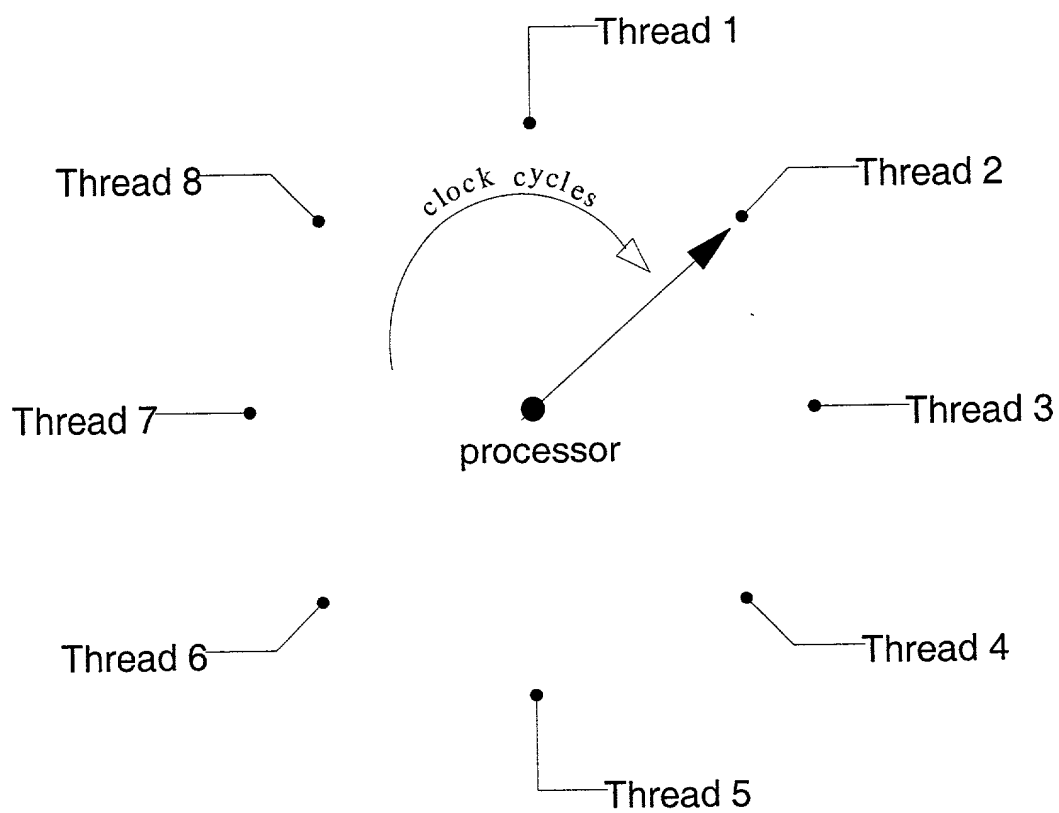


Figure 2

Figure 3a: Four-Thread Processor. This diagram illustrates the state of a four-thread processor over 16 clock cycles. The processor has four threads (1A, 2A, 3A, 4A) and four stages (PC, FETCH, DECODE, OPERAND, EXECUTE, ADDRESS, MEM, WRITEBACK). The state is shown in a grid where each cell contains the thread ID and the stage it is currently in.

Four-Thread Processor

active thread	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
PC	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
FETCH		1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E
DECODE			1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E
OPERAND				1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E
EXECUTE					1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D
ADDRESS						1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D
MEM							1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D
MEM								1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D
MEM									1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C
WRITEBACK										1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C
memory in use																				

Figure 3a

Four-Thread Processor with Banked Memory

active thread	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
PC	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
FETCH		1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E
DECODE			1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E
OPERAND				1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E
EXECUTE					1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D
ADDRESS						1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D
MEM							1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D
MEM								1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D
MEM									1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C
WRITEBACK										1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C
memory1 in use																				
memory2 in use																				

Figure 3b

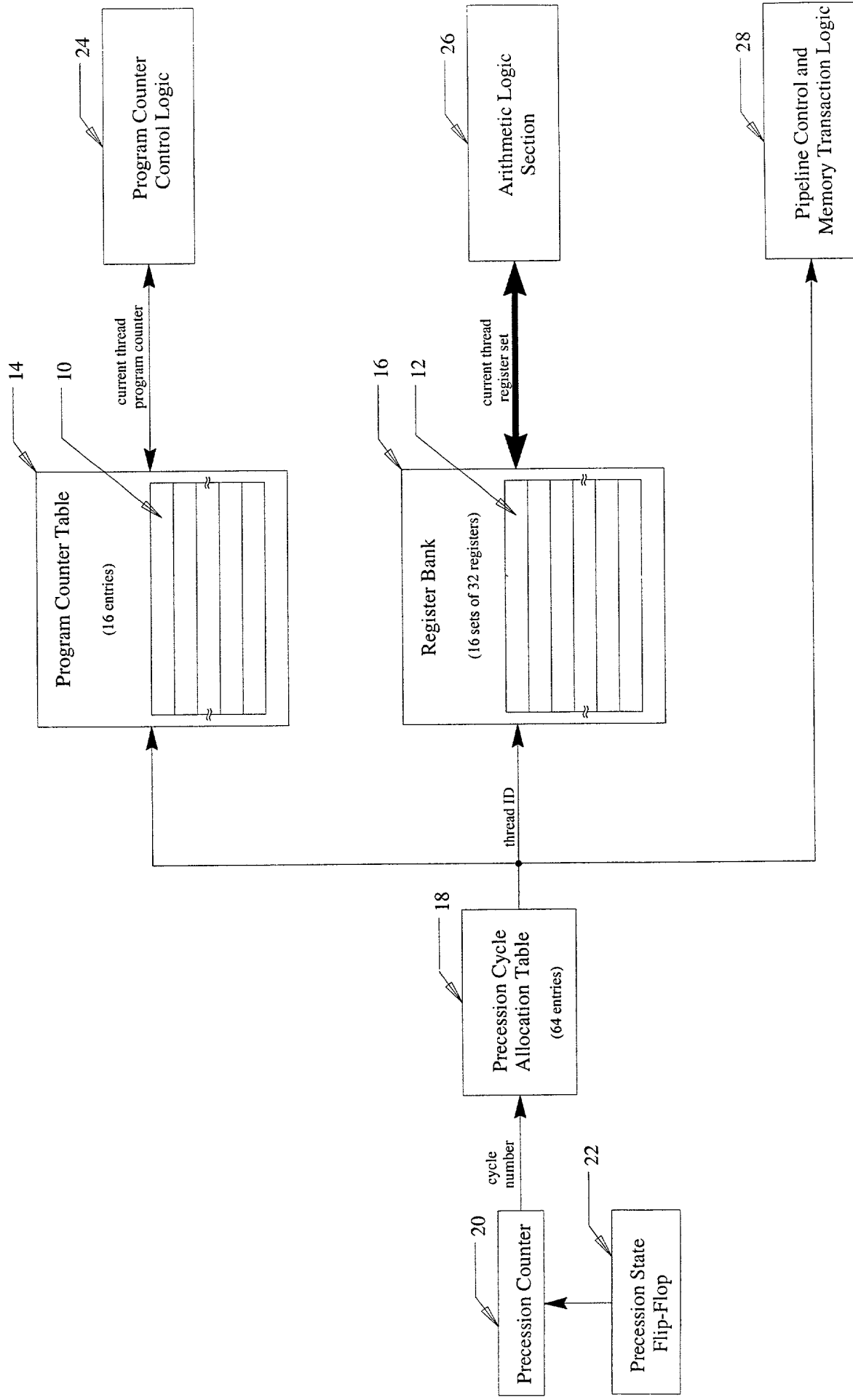


Figure 4

Cycle Allocation Table

- 1
- 2
- 3
- 4
- 5
- 6
- 7
- 8
- 9
- 10
- 11
- 12
- 13
- 14
- 15
- 16
- 1
- 2
- 3
- 4
- 5
- 6
- 7
- 8
- 9
- 10
- 11
- 12
- 13
- 14
- 15
- 16
- ...
- ...

commutator

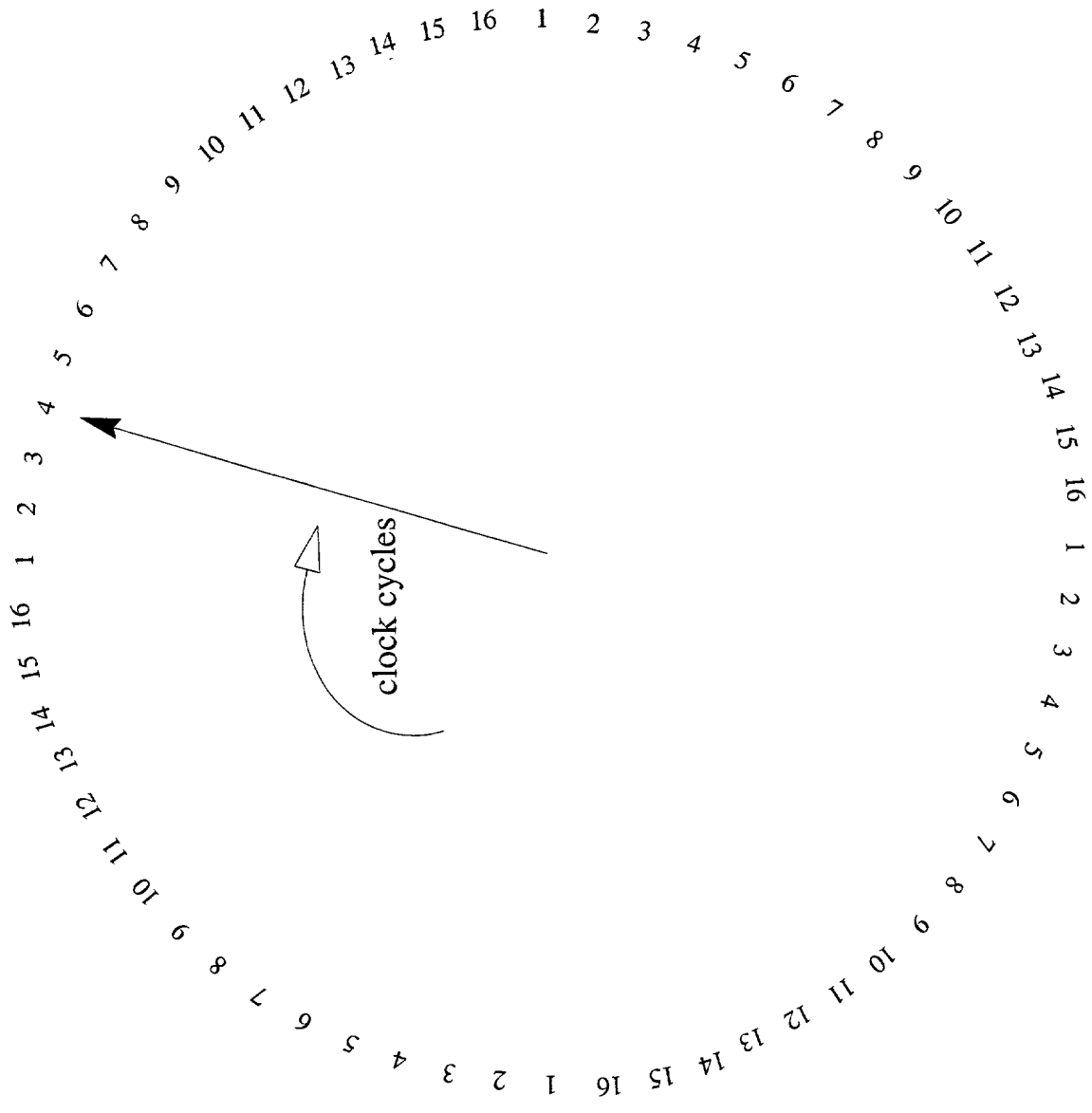


Figure 5

Figure 6: Cycle Allocation Table

Cycle Allocation Table

commutator

